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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/667,528	09/22/2000	Raimund Sonning	2789-26	9877

23117 7590 09/14/2005

NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER	
BAYARD, EMMANUEL	
ART UNIT	**PAPER NUMBER**
2638	

DATE MAILED: 09/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/667,528	SONNING ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2638	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *9,10,23 and 24* is/are allowed.

6)☒ Claim(s) *1-8,11-22 and 25-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is in response to amendment filed on 6/29/05 in which claims 1-34 are pending. The applicant's arguments have been fully considered but they are moot based on the new ground of rejection.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, 4, 6-7, 11-12, 13, 15, 17-19, 25, 28, 30-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Shiomoto et al U.S. Pub No 20020053049 A1.

As per claims 1, 11, 13, 18-19 Shimoto et al teaches an interleaver of a transmitter for interleaving input data bit sequences (BS) of M data bits comprising code symbols each consisting of a number N of data bits and control information associated with every code symbol to be used to control processing in said transmitter and consisting of a number L of control bits indicating specific states for each corresponding code symbol comprising: an encoding section is

the same as the claimed (channel encoder) (see figs.7, 8 elements 30a, 30b and page 2, paragraph [0036-0038]) for receiving digital data in the form of packets from a data source and for encoding said digital data into said channel encoded code symbols of said number N of data bits; a multiplexer for adding is the same as the claimed (combining means for combining) (see figs. 7, 8 element 34 and page 3, paragraph [0043]) the respective data bits of each code symbol with the associated L control bits into a control information/ code (see figs. 7, 8 element S40 and page 2, paragraph [0037-0038]) symbol data word of L + N bits; control information/code symbol **encoding means** (see figs.7, 8 element 36 and page 3, paragraph [0044]) for encoding said L + N bit control information/code symbol data words into data words of K bits, where K<L + N, according to a predetermined encoding scheme; an interleaving memory for storing (see figs. 7, 8 element 41 and page 3, paragraph [0045]) said encoded data words at memory locations thereof.

As per claims 4, 17 Shimoto et al inherently teaches on control bit indicates a transmission power on/off.

As per claim 6, the interleaver of Shimoto does teach a convolutional encoding having a coding rate (see paragraph [0009]).

As per claim 7, the interleaver of Shimoto does teach interleaving memory (see figs. 7, 8 element 41 and page 3, paragraph [0045]). Therefore the memory inherently includes number of rows and columns.

As per claim 12, the transmitter of Shimoto does teach a modulation means (see fig.7 element 43).

As per claim 15, the method of Shimoto does include a processing decoded code (see fig.21 element 115).

As per claims 25 and 33, Shimoto et al teaches an interleaver of a transmitter for interleaving input data bit sequences (BS) of M data bits comprising code symbols each consisting of a number N of data bits and control information associated with every code symbol to be used to control processing in said transmitter and consisting of a number L of control bits indicating specific states for each corresponding code symbol comprising: a channel coder is the same as the claimed (channel encoder) (see figs.7, 8 elements 30a, 30b and page 2, paragraph [0036-0038]) for receiving digital data in the form of packets from a data source and for encoding said digital data into said channel encoded code symbols of said number N of data bits; a multiplexer for adding is the same as the claimed (combining means for combining) (see figs. 7, 8 element 34 and page 3, paragraph [0043]) the respective data bits of each code symbol with the associated L control bits into a control information/ code (see figs. 7, 8 element S40 and page 2, paragraph [0037-0038]) symbol data word of L + N bits; control information/code symbol **encoding means** (see figs.7, 8 element 36 and page 3, paragraph [0044]) for encoding said L + N bit control information/code symbol data words into data words of K bits, where K<L + N, according to a predetermined encoding scheme; an interleaving memory for (see figs. 7, 8 element 41 and page 3, paragraph [0045]) said encoded data words at memory locations thereof; a decoder (see fig.20 element 120 and page 8, paragraph [0085]) which derives the control information from the data words; a radio

frequency transmitter element (see, paragraphs [0037-0038], [0048], [0085]) whose operation is controlled by the controlled information derived from the decoder.

As per claim 28 Shimoto et al inherently teaches on control bit indicates a transmission power on/off.

As per claim 30 the interleaver of Shimoto does teach a convolutional encoding having a coding rate (see paragraph [0009]).

As per claim 31 the interleaver of Shimoto does teach interleaving memory (see figs. 7, 8 element 41 and page 3, paragraph [0045]). Therefore the memory inherently includes number of rows and columns.

As per claims 32 and 34 the method of Shimoto does include a radio frequency transmitter (see paragraph [0048]).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2-3, 5, 8, 14, 16, 20-22, 26-27, 29 rejected under 35 U.S.C. 103(a) as being unpatentable over Shiomoto et al U.S. Pub No 20020053049 A1 in view of Hatakeyama et al U.S. patent No 6,507,629 B1.

As per claims 2, 8, 14, 26 Shimoto teaches all the features of the claimed invention except write/read means for writing said encoded data to an interleaving matrix having row and column directions.

Hatakeyama teaches teach write/read means in row and column directions (see abstract and figs.8, 9, 14, 17 elements 51, 52, 6, 10 and col. 12, lines 48-55 and col. 14, lines 10, 22 and col. 15, line 48 and col. 17, lines 15-20 and col.21, lines 53-58 and col.22, lines 2-6, 21-25) and symbol decoding means (see fg.4 elements 13, 27 and co1.9, line 41 and col. 10, line 12). Note that a matrix is known in the art as function having Rows and column. Since the interleaver of Hatakemaya teaches Rows and column therefore the interleaving Matrix is inherently taught by Hatakemaya.

It would have been obvious to one of ordinary skill in the art to implement the teaching of Hatakeyama into Shimoto as to reduce the memory capacity required to for interleave processing as taught by Hatakeyama (see col.4. lines 19-20).

As per claims 3, 16 and 27 the interleaving of Hatakemaya does teach a frame start, a power bit (seecol.3, lines 52-69 and co1.24, lines 17-20, 50-55). Note that a frame is known in the art as plurality of time slot having a header, a maker. Since Hatakemaya teaches a frame function therefore the time slot start and a marker is inherently taught by Hatakemaya. Furthermore implementing such teaching into Shimoto would have been obvious to one skilled in the art as to reduce the memory capacity required to for interleave processing as taught by Hatakeyama (see col.4. lines 19-20).

As per claims 5, 29, the interleaver of Hatakemaya does teach a selection means of write/read means (see abstract). Furthermore implementing such teaching into each memory location of Shimoto reference would have been obvious to one skilled in the art as to reduce the memory capacity required to for interleave processing as taught by Hatakeyama (see col.4. lines 19-20).

As per claims 20-22, Shimoto teaches all the features of the claimed invention (see claims 1 and 25 above) except write/read means for writing said encoded data to an interleaving matrix within said interleaving memory at specific memory location in a row direction and for reading out said encoded data words from said interleaving matrix in the column direction.

Hatakeyama teaches teach write/read means in row and column directions (see abstract and figs.8, 9, 14, 17 elements 51, 52, 6, 10 and col. 12, lines 48-55 and col. 14, lines 10, 22 and col. 15, line 48 and col. 17, lines 15-20 and col.21, lines 53-58 and col.22, lines 2-6, 21-25) and symbol decoding means (see fg.4 elements 13, 27 and co1.9, line 41 and col. 10, line 12). Note that a matrix is known in the art as function having Rows and column. Since the interleaver of Hatakemaya teaches Rows and column therefore the interleaving Matrix is inherently taught by Hatakemaya.

It would have been obvious to one of ordinary skill in the art to implement the teaching of Hatakeyama into Shimoto as to reduce the memory capacity required to for interleave processing as taught by Hatakeyama (see col.4. lines 19-20).

Allowable Subject Matter

Claims 9-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 23-24 are allowed over the prior art of record.

The following is a statement of reasons for the indication of allowable subject matter: a shift means for shifting the register (ro, r1) which was read at the last write cycle and the second registers of the register banks (b0, b1) while reading in the next odd and even bits of a next input data bit sequence to the respective second register (r1) of each register bank as recited in claims 8-10 and 23-24.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wolf U.S. Patent No 5,983,383 teaches a method and apparatus for transmitting and receiving.

Dorward et al U.S. Patent No 5,463,641 teaches a tailored error protection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vanderpuye Kenneth can be reached on 571 272 3078.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2638

9/9/05

EMMANUEL BAYARD
PRIMARY EXAMINER